Listing of Claims

1. (Currently Amended) A silicon carbide metal-oxide semiconductor field effect transistor, comprising:

a double implant silicon carbide MOSFET, having an n-type silicon carbide drift layer, spaced apart p-type silicon carbide regions in the n-type silicon carbide drift layer and having n-type silicon carbide regions therein, and a nitrided oxide layer on the n-type silicon carbide drift layer; and

n-type shorting channels extending from respective ones of the n-type silicon carbide regions through the p-type silicon carbide regions and to the n-type silicon carbide drift layer, wherein the n-type shorting channels extend to but not into the n-type silicon carbide drift layer and wherein the n-type shorting channels have a higher n-type dopant concentration than is present in a region disposed between the n-type shorting channels.

2. (Original) A silicon carbide metal-oxide semiconductor field effect transistor according to Claim 1, wherein the p-type silicon carbide regions comprise spaced apart regions of silicon carbide having aluminum implanted therein.

3. Cancelled.

4. (Currently Amended) A silicon carbide metal-oxide semiconductor field effect transistor, comprising:

a double implant silicon carbide MOSFET, having an n-type silicon carbide drift layer, spaced apart p-type silicon carbide regions in the n-type silicon carbide drift layer and having n-type silicon carbide regions therein, and a nitrided oxide layer on the n-type silicon carbide drift layer;~~and~~

n-type shorting channels extending from respective ones of the n-type silicon carbide regions through the p-type silicon carbide regions and to the n-type silicon carbide drift layer, the n-type shorting channels extending to but not beyond a periphery of the p-type silicon carbide regions and wherein the n-type shorting

<u>channels have a higher n-type dopant concentration than is present in a region disposed between the n-type shorting channels; and</u>

an epitaxial layer of silicon carbide on the n-type silicon carbide drift layer between the n-type shorting channels.

5. (Original) A silicon carbide metal-oxide semiconductor field effect transistor according to Claim 1, further comprising a gate contact on the oxide layer, the gate contact comprising p-type polysilicon.

6. (Original) A silicon carbide metal-oxide semiconductor field effect transistor according to Claim 1, wherein the n-type shorting channels are doped so that the n-type channels are self depleted when a zero volt gate bias is applied.

7. Cancelled.

8. (Original) A silicon carbide metal-oxide field effect transistor according to Claim 1, wherein the shorting channels have a sheet charge of less than about 10^{13} cm^{-2}.

9. (Original) A silicon carbide metal-oxide field effect transistor according to Claim 1, wherein the shorting channels have a sheet charge corresponding to a silicon carbide epitaxial layer having a thickness of about 3500 Å and a carrier concentration of about 2×10^{16} cm^{-3}.

10. (Original) A silicon carbide metal-oxide field effect transistor according to Claim 1, wherein the silicon carbide comprises 4H polytype silicon carbide and wherein an interface between the oxide layer and the n-type drift layer has an interface state density of less than 10^{12} $eV^{-1}cm^{-2}$ for energy levels between about 0.3 and about 0.4 eV of a conduction band energy of 4H polytype silicon carbide.

11. (Original) A silicon carbide metal-oxide field effect transistor according to Claim 1, wherein the nitride oxide comprises at least one of an oxide-nitride-oxide structure and an oxynitride.

12. (Currently Amended) A silicon carbide device comprising:

a drift layer of n-type silicon carbide;

first regions of p-type silicon carbide in the drift layer, the first regions of p-type silicon carbide being spaced apart and having peripheral edges which define a region of the drift layer therebetween;

first regions of n-type silicon carbide having a carrier concentration greater than a carrier concentration of the drift layer in the first regions of p-type silicon carbide and spaced apart from the peripheral edges of the first regions of p-type silicon carbide;

second regions of n-type silicon carbide having a carrier concentration less than the carrier concentration of the first regions of n-type silicon carbide and which extend from the first regions of n-type silicon carbide to, but not substantially beyond, the peripheral edges of the first regions of p-type silicon carbide and wherein the second regions of n-type silicon carbide have a higher n-type dopant concentration than is present in a region disposed between the second regions of n-type silicon carbide; and

a nitrided oxide layer on the drift layer, the first regions of n-type silicon carbide and the second regions of n-type silicon carbide.

13. (Original) A silicon carbide device according to Claim 12, wherein the second regions of n-type silicon carbide have a sheet charge of less than about 10^{13} cm^{-2}.

14. (Original) A silicon carbide device according to Claim 13, wherein the second regions of n-type silicon carbide have a depth of from about 0.05 μm to about 1 μm.

15. (Previously Presented) A silicon carbide device comprising:

a drift layer of n-type silicon carbide;

first regions of p-type silicon carbide in the drift layer, the first regions of p-type silicon carbide being spaced apart and having peripheral edges which define a region of the drift layer therebetween;

first regions of n-type silicon carbide having a carrier concentration greater than a carrier concentration of the drift layer in the first regions of p-type silicon carbide and spaced apart from the peripheral edges of the first regions of p-type silicon carbide;

second regions of n-type silicon carbide having a carrier concentration less than the carrier concentration of the first regions of n-type silicon carbide and which extend from the first regions of n-type silicon carbide to the peripheral edges of the first regions of p-type silicon carbide;

a nitrided oxide layer on the drift layer, the first regions of n-type silicon carbide and the second regions of n-type silicon carbide; and

wherein the second regions of n-type silicon carbide extend a distance of from about 0.5 μm to about 5 μm from the first regions of n-type silicon carbide to the peripheries of the first regions of p-type silicon carbide.

16. (Original) A silicon carbide device according to Claim 12, wherein the second regions of n-type silicon carbide have a sheet charge corresponding to a silicon carbide epitaxial layer having a thickness of about 3500 Å and a carrier concentration of about 2×10^{16} cm^{-3}.

17. (Original) A silicon carbide device according to Claim 12, wherein an interface state density of an interface between the oxide layer and the drift layer, the first regions of n-type silicon carbide and the second regions of n-type silicon carbide is less than about 10^{12} $eV^{-1}cm^{-2}$ between about 0.3 and about 0.4 eV of the conduction band energy of 4H polytype silicon carbide.

18. (Original) A silicon carbide device according to Claim 12, further comprising second regions of p-type silicon carbide disposed in respective ones of the first regions of p-type silicon carbide, wherein the second regions of p-type silicon carbide have a carrier concentration greater than the carrier concentration of the first regions of silicon carbide, the second regions of silicon carbide being adjacent the first regions of n-type silicon carbide and opposite the second regions of n-type silicon carbide.

19. (Original) A silicon carbide device according to Claim 12, further comprising a gate contact on the oxide layer.

20. (Original) A silicon carbide device according to Claim 19, wherein the gate contact is p-type polysilicon.

21. (Previously Presented) A silicon carbide device, comprising:

a drift layer of n-type silicon carbide;

first regions of p-type silicon carbide in the drift layer, the first regions of p-type silicon carbide being spaced apart and having peripheral edges which define a region of the drift layer therebetween;

first regions of n-type silicon carbide having a carrier concentration greater than a carrier concentration of the drift layer in the first regions of p-type silicon carbide and spaced apart from the peripheral edges of the first regions of p-type silicon carbide;

second regions of n-type silicon carbide having a carrier concentration less than the carrier concentration of the first regions of n-type silicon carbide and which extend from the first regions of n-type silicon carbide to the peripheral edges of the first regions of p-type silicon carbide;

a nitrided oxide layer on the drift layer, the first regions of n-type silicon carbide and the second regions of n-type silicon carbide; and

wherein the first regions of p-type silicon carbide are spaced apart by a distance of from about 1 μm to about 10 μm.

22. (Original) A silicon carbide device according to Claim 21, wherein the first regions of p-type silicon carbide have a carrier concentration of from about 1×10^{16} to about 2×10^{19} cm^{-3}.

23. (Original) A silicon carbide device according to Claim 12, further comprising contacts on the first region of p-type silicon carbide and the first region of n-type silicon carbide.

24. (Original) A silicon carbide device according to Claim 12, further comprising:

a layer of n-type silicon carbide having a carrier concentration greater than the carrier concentration of the drift layer and disposed adjacent the drift layer opposite the oxide layer; and

a drain contact on the layer of n-type silicon carbide.

25. (Original) A silicon carbide device according to Claim 12, further comprising an epitaxial layer of silicon carbide on the first p-type regions and the drift layer of n-type silicon carbide, wherein the second regions of n-type silicon carbide extend into the epitaxial layer, the first regions of n-type silicon carbide extend through the epitaxial layer and the oxide layer is on the epitaxial layer, the first regions of n-type silicon carbide and the second regions of n-type silicon carbide.

26. (Previously Presented) A silicon carbide device, comprising:

a drift layer of n-type silicon carbide;

first regions of p-type silicon carbide in the drift layer, the first regions of p-type silicon carbide being spaced apart and having peripheral edges which define a region of the drift layer therebetween;

first regions of n-type silicon carbide having a carrier concentration greater than a carrier concentration of the drift layer in the first regions of p-type silicon

carbide and spaced apart from the peripheral edges of the first regions of p-type silicon carbide;

second regions of n-type silicon carbide having a carrier concentration less than the carrier concentration of the first regions of n-type silicon carbide and which extend from the first regions of n-type silicon carbide to the peripheral edges of the first regions of p-type silicon carbide;

a nitrided oxide layer on the drift layer, the first regions of n-type silicon carbide and the second regions of n-type silicon carbide;

an epitaxial layer of silicon carbide on the first p-type regions and the drift layer of n-type silicon carbide, wherein the second regions of n-type silicon carbide extend into the epitaxial layer, the first regions of n-type silicon carbide extend through the epitaxial layer and the oxide layer is on the epitaxial layer, the first regions of n-type silicon carbide and the second regions of n-type silicon carbide; and

wherein the epitaxial layer comprises undoped silicon carbide.

27. (Original) A silicon carbide device according to Claim 25, wherein the epitaxial layer of silicon carbide comprises an epitaxial layer of silicon carbide having a thickness of from about 0.05 μm to about 1 μm.

28. (Original) A silicon carbide device according to Claim 27, wherein the epitaxial layer of silicon carbide comprises an epitaxial layer of silicon carbide having a thickness of from about 1000 to about 5000 Å.

29. (Original) A silicon carbide device according to Claim 25, wherein the epitaxial layer comprises n-type silicon carbide having a sheet charge of less than about 10^{13} cm^{-2}.

30. (Original) A silicon carbide device according to Claim 25, wherein the second regions of n-type silicon carbide have a sheet charge of less than about 10^{13} cm^{-2}.

31. (Original) A silicon carbide device according to Claim 30, wherein the second regions of n-type silicon carbide have a depth of from about 0.05 μm to about 1 μm.

32. (Previously Presented) A silicon carbide device, comprising:

a drift layer of n-type silicon carbide;

first regions of p-type silicon carbide in the drift layer, the first regions of p-type silicon carbide being spaced apart and having peripheral edges which define a region of the drift layer therebetween;

first regions of n-type silicon carbide having a carrier concentration greater than a carrier concentration of the drift layer in the first regions of p-type silicon carbide and spaced apart from the peripheral edges of the first regions of p-type silicon carbide;

second regions of n-type silicon carbide having a carrier concentration less than the carrier concentration of the first regions of n-type silicon carbide and which extend from the first regions of n-type silicon carbide to the peripheral edges of the first regions of p-type silicon carbide;

a nitrided oxide layer on the drift layer, the first regions of n-type silicon carbide and the second regions of n-type silicon carbide;

an epitaxial layer of silicon carbide on the first p-type regions and the drift layer of n-type silicon carbide, wherein the second regions of n-type silicon carbide extend into the epitaxial layer, the first regions of n-type silicon carbide extend through the epitaxial layer and the oxide layer is on the epitaxial layer, the first regions of n-type silicon carbide and the second regions of n-type silicon carbide; and

wherein the second regions of n-type silicon carbide extend a distance of from about 0.5 μm to about 5μm from the first regions of n-type silicon carbide to the peripheries of the first regions of p-type silicon carbide.

33. (Original) A silicon carbide device according to Claim 25, wherein an interface state density of an interface between the oxide layer and the epitaxial layer, the first regions of n-type silicon carbide and the second regions of n-type

silicon carbide is less than about 10^{12} $eV^{-1}cm^{-2}$ between about 0.3 and about 0.4 eV of the conduction band energy of 4H polytype silicon carbide.

34. (Original) A silicon carbide device according to Claim 25, further comprising second regions of p-type silicon carbide disposed in respective ones of the first regions of p-type silicon carbide, wherein the second regions of p-type silicon carbide have a carrier concentration greater than the carrier concentration of the first regions of silicon carbide, the second regions of silicon carbide being adjacent the first regions of n-type silicon carbide and opposite the second regions of n-type silicon carbide.

35. (Original) A silicon carbide device according to Claim 34, further comprising:

windows in the epitaxial layer positioned to expose the second regions of p-type silicon carbide; and

first source contacts within the window on the second regions of p-type silicon carbide and on the first regions of n-type silicon carbide.

36. (Original) A silicon carbide device according to Claim 25, further comprising a gate contact on the oxide layer.

37. (Original) A silicon carbide device according to Claim 36, wherein the gate contact is p-type polysilicon.

38. (Previously Presented) A silicon carbide device, comprising:

a drift layer of n-type silicon carbide;

first regions of p-type silicon carbide in the drift layer, the first regions of p-type silicon carbide being spaced apart and having peripheral edges which define a region of the drift layer therebetween;

first regions of n-type silicon carbide having a carrier concentration greater than a carrier concentration of the drift layer in the first regions of p-type silicon

carbide and spaced apart from the peripheral edges of the first regions of p-type silicon carbide;

second regions of n-type silicon carbide having a carrier concentration less than the carrier concentration of the first regions of n-type silicon carbide and which extend from the first regions of n-type silicon carbide to the peripheral edges of the first regions of p-type silicon carbide;

a nitrided oxide layer on the drift layer, the first regions of n-type silicon carbide and the second regions of n-type silicon carbide;

an epitaxial layer of silicon carbide on the first p-type regions and the drift layer of n-type silicon carbide, wherein the second regions of n-type silicon carbide extend into the epitaxial layer, the first regions of n-type silicon carbide extend through the epitaxial layer and the oxide layer is on the epitaxial layer, the first regions of n-type silicon carbide and the second regions of n-type silicon carbide; and

wherein the first regions of p-type silicon carbide are spaced apart by a distance of from about 1μm to about 10μm.

39. (Original) A silicon carbide device according to Claim 38, wherein the first regions of p-type silicon carbide have a carrier concentration of from about 1×10^{16} to about 2×10^{19} cm^{-3}.

40. (Original) A silicon carbide device according to Claim 25, further comprising:

a layer of n-type silicon carbide having a carrier concentration greater than the carrier concentration of the drift layer and disposed adjacent the drift layer opposite the oxide layer; and

a drain contact on the layer of n-type silicon carbide.

41. (Original) A silicon carbide metal-oxide field effect transistor according to Claim 12, wherein the nitride oxide layer comprises at least one of an oxide-nitride-oxide structure and an oxynitride layer.

42 - 82. Cancelled.

83. (Currently Amended) A silicon carbide metal-oxide semiconductor field effect transistor, comprising:

a silicon carbide MOSFET, having an n-type silicon carbide drift layer, spaced apart p-type silicon carbide regions in the n-type silicon carbide drift layer and having n-type silicon carbide regions therein, and a nitrided oxide layer on the n-type silicon carbide drift layer;

a region between the n-type silicon carbide regions and the drift layer and is adjacent the nitrided oxide layer that is configured to self deplete upon application of a zero gate bias; and

wherein the region that is configured to self-deplete extends to but not into the n-type silicon carbide drift layer and has a higher n-type dopant concentration than is present in an n-type silicon carbide region adjacent the region that is configured to self deplete.

84. (Original) A silicon carbide metal-oxide semiconductor field effect transistor according to Claim 83, wherein the p-type silicon carbide regions comprise spaced apart regions of silicon carbide having aluminum implanted therein.

85. Cancelled.

86. Cancelled.

87. (Original) A silicon carbide metal-oxide semiconductor field effect transistor according to Claim 83, wherein the region that is configured to self-deplete comprises a region of silicon carbide having a sheet charge corresponding to a sheet charge of an epitaxial layer of silicon carbide having a thickness of about 3500 Å and carrier concentration of about 2×10^{16} cm^{-3}.

88. (Original) A silicon carbide metal-oxide semiconductor field effect transistor according to Claim 83, further comprising a gate contact on the oxide layer, the gate contact comprising p-type polysilicon.

89. (Original) A silicon carbide metal-oxide field effect transistor according to Claim 83, wherein the silicon carbide comprises 4H polytype silicon carbide and wherein an interface between the oxide layer and the n-type drift layer has an interface state density of less than 10^{12} $eV^{-1}cm^{-2}$ for energy levels between about 0.3 and about 0.4 eV of a conduction band energy of 4H polytype silicon carbide.

90. Cancelled.